USER'S GUIDE

QUADRASYNC/C

Model 10022

May 6, 1977

ABLE COMPUTER TECHNOLOGY, Inc.

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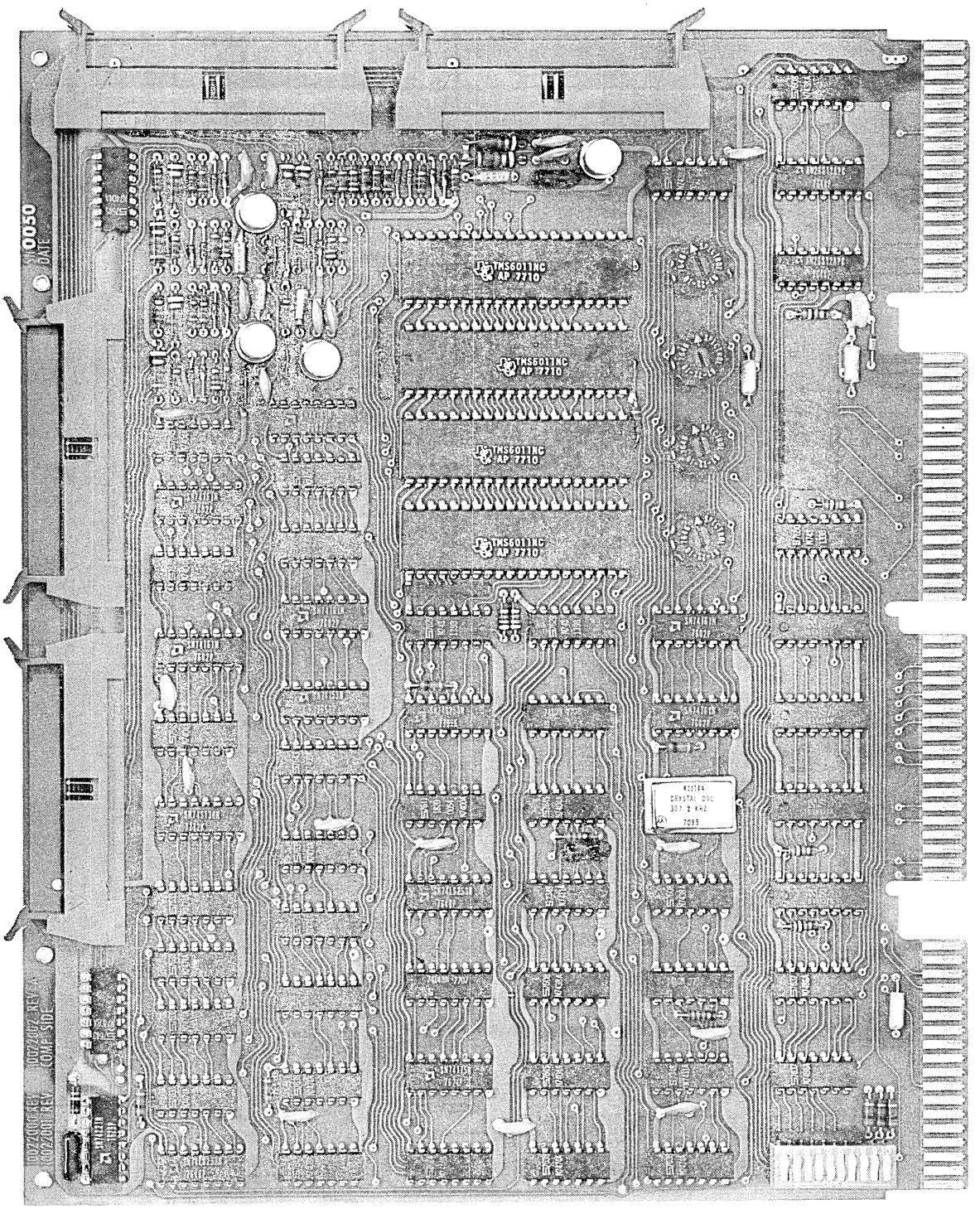


QuadrAsync/C - Model 10022

FUNCTION

Provides an interface between the PDP*-11 UNIBUS* and four asynchronous 20 mA Communication Channels. Software compatible with the Digital Equipment Corporation DL-11C.

MECHANICAL

The QUADRASYNC/C** consists of one quad module which can be installed in any Small Peripheral Controller (SPC) slot.

OPERATING MODE

Full-duplex or half-duplex communication capability the same as furnished with the DEC* Model DL-11C.

DATA FORMAT

Asynchronous, 20 mA current loop. One start bit, 8 data bits and one stop bit. Low order bit first.

BUS LOADING

The QUADRASYNC/C presents one unit load to the UNIBUS.

ELECTRICAL INTERFACE

The QUADRASYNC/C provides 20 mA active current loop for both send and receive leads for connection to local teleprinters such as DIGITAL LA30 and LA36 and displays such as DIGITAL VT05 terminal.

POWER REQUIREMENTS

2.150 amps @ + 5V
0.300 amps @ - 15V

DATA RATES

The QUADRASYNC/C offers seven independently selectable baud rates for each channel. The transmitter and receiver of each channel operate at the identical baud rate. The baud rates are:

BAUD RATE	SWITCH POSITION
9600 baud	7
4800 baud	6
2400 baud	5
1200 baud	4
600 baud	3
300 baud	2
150 baud	1

NOTES:

1) Switch position 1 is when the arrow ON switch is pointed directly toward UART.

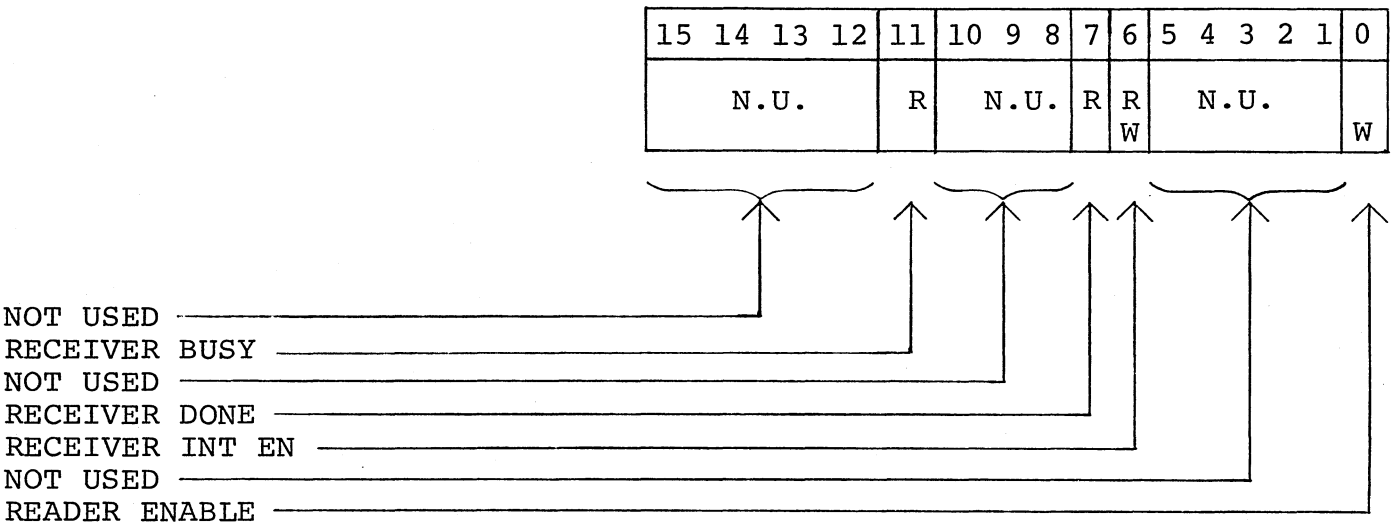
2) Ascending positions are in clockwise direction.

3) CH 1 switch is closest to center of board and ascending to CH 4 on left side of board.

PROGRAMMING SPECIFICATIONS

RECEIVER STATUS REGISTERS: 77XXX0

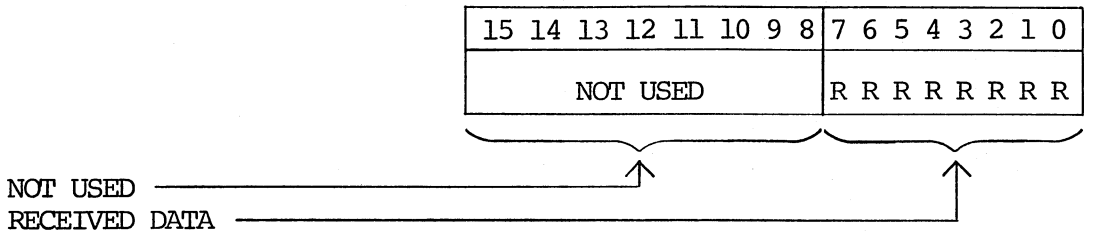
Receiver Status Register	#1 X00
Receiver Status Register	#2 X01
Receiver Status Register	#3 X10
Receiver Status Register	#4 X11



BIT	DESCRIPTION AND OPERATION
15-12	NOT USED. READ AS ZERO.
11	READ ONLY. SET WHEN UART RECEIVES VALID START BIT. CLEARED BY BIT 7 WHEN SET, AND BY INIT.
10-8	NOT USED. READ AS ZERO.
7	READ ONLY. SET WHEN UART HAS INCOMING DATA ASSEMBLED AND READY FOR TRANSFER. CLEARED BY SETTING BIT 0 (READER ENABLE), ADDRESSING READER BUFFER, OR BY INIT.
6	READ/WRITE. WHEN SET CAUSES AN INTERRUPT REQUEST EACH TIME BIT 7 (RECEIVER DONE IS SET). CLEARED BY PROGRAM OR INIT.
5-1	NOT USED. READ AS ZERO.
0	WRITE ONLY. READ AS ZERO. WHEN SET, CLEARS BIT 7 (RECEIVER DONE). THIS BIT DOES NOT CONTROL A READER RUN RELAY TO ADVANCE THE PAPER TAPE READER AS ON CERTAIN DIGITAL SUPPLIED TELEPRINTERS.

RECEIVER DATA BUFFER REGISTERS: 77XXX2

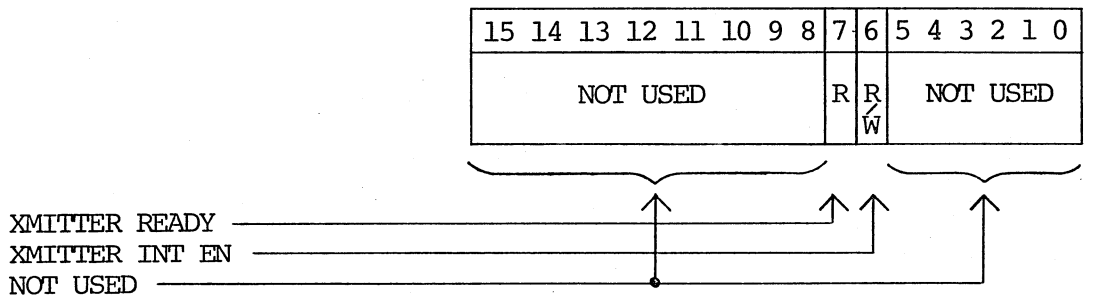
Receiver Data Buffer	#1 X00
Receiver Data Buffer	#2 X01
Receiver Data Buffer	#3 X10
Receiver Data Buffer	#4 X11



BIT	DESCRIPTION AND OPERATION
15-8	NOT USED. READ AS ZERO.
7-0	RECEIVED DATA. READ ONLY. LAST COMPLETE CHARACTER ASSEMBLED BY THE UART. CHARACTERS ARE RIGHT JUSTIFIED WHEN CHARACTERS ARE LESS THAN 8 BITS.

TRANSMITTER STATUS REGISTERS: 77XXX4

Transmitter Status	#1 X00
Transmitter Status	#2 X01
Transmitter Status	#3 X10
Transmitter Status	#4 X11



BIT	DESCRIPTION AND OPERATION
15-8	NOT USED. READ AS ZERO.
7	READ ONLY. SET WHEN TRANSMITTER CAN ACCEPT ANOTHER CHARACTER AND BY INIT. CLEARED WHEN A CHARACTER IS LOADED INTO THE TRANSMITTER BUFFER.
6	READ/WRITE. WHEN SET, WILL CAUSE AN INTERRUPT REQUEST WHENEVER BIT 7 IN THE TRANSMITTER STATUS REGISTER IS SET. CLEARED BY THE PROGRAM AND BY INIT.
5-0	NOT USED. READ AS ZERO.

TRANSMITTER BUFFER REGISTERS: 77XXX6

Transmitter Buffer	#1 X00
Transmitter Buffer	#2 X01
Transmitter Buffer	#3 X10
Transmitter Buffer	#4 X11

15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
NOT USED	W W W W W W W W

NOT USED
TRANSMITTER DATA

BIT	DESCRIPTION AND OPERATION
7-0	WRITE ONLY. CONTAINS THE CHARACTER TO BE TRANSMITTED BY THE UART. WHEN FEWER THAN 8 DATA BITS, THE CHARACTER MUST BE RIGHT JUSTIFIED WHEN LOADED INTO THE TRANSMITTER BUFFER. A BIT SET WILL CAUSE A MARK TO APPEAR ON THE TRANSMITTED DATA LEAD FOR ONE BIT TIME. CLEARED BY INIT.

ADDRESS SELECTION									SW 4	SW 2	SW 5	SW 1	SW 6	SW 3				ADDRESS SWITCH SELECTION
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	REGISTER
1	1	1	1	1	1	1	X	X	X	X	X	X	0	0	0	0	0	R C S R #1
1	1	1	1	1	1	1	X	X	X	X	X	X	0	0	0	1	0	R B U F #1
1	1	1	1	1	1	1	X	X	X	X	X	X	0	0	1	0	0	X C S R #1
1	1	1	1	1	1	1	X	X	X	X	X	X	0	0	1	1	0	X B U F #1
1	1	1	1	1	1	1	X	X	X	X	X	X	0	1	0	0	0	R C S R #2
1	1	1	1	1	1	1	X	X	X	X	X	X	0	1	0	1	0	R B U F #2
1	1	1	1	1	1	1	X	X	X	X	X	X	0	1	1	0	0	X C S R #2
1	1	1	1	1	1	1	X	X	X	X	X	X	0	1	1	1	0	X B U F #2
1	1	1	1	1	1	1	X	X	X	X	X	X	1	0	0	0	0	R C S R #3
1	1	1	1	1	1	1	X	X	X	X	X	X	1	0	0	1	0	R B U F #3
1	1	1	1	1	1	1	X	X	X	X	X	X	1	0	1	0	0	X C S R #3
1	1	1	1	1	1	1	X	X	X	X	X	X	1	0	1	1	0	X B U F #3
1	1	1	1	1	1	1	X	X	X	X	X	X	1	1	0	0	0	R C S R #4
1	1	1	1	1	1	1	X	X	X	X	X	X	1	1	0	1	0	R B U F #4
1	1	1	1	1	1	1	X	X	X	X	X	X	1	1	1	0	0	X C S R #4
1	1	1	1	1	1	1	X	X	X	X	X	X	1	1	1	1	0	X B U F #4

SW - OPEN = 0
SW - CLOSED = 1

ADDRESS RANGE: 777776, 777676, 776500 } DL11-A,-B
776176, 775610, 774000 } DL11-C,-D,-E

ADDRESS IS NORMALLY SET FOR 776500 176540

VECTOR ADDRESS: 340

SW 7	SW 10	SW 9	SW 8	SWITCH SELECTION					
8	7	6	5	4	3	2	1	0	VECTOR
X	X	X	X	0	0	0	0	0	RCVR #1
X	X	X	X	0	0	1	0	0	XMIT #1
X	X	X	X	0	1	0	0	0	RCVR #2
X	X	X	X	0	1	1	0	0	XMIT #2
X	X	X	X	1	0	0	0	0	RCVR #3
X	X	X	X	1	0	1	0	0	XMIT #3
X	X	X	X	1	1	0	0	0	RCVR #4
X	X	X	X	1	1	1	0	0	XMIT #4

SW - OPEN = 1
SW - CLOSED = 0

VECTOR ADDRESSES ARE NORMALLY SET TO
774 thru 740

VECTOR RANGE:

7 7 4 thru 0 0 0 STARTING FROM 000_8 AND IN INCREMENTS OF 040_8.

CONNECTOR LIST

J1

BERG PIN NO.	SIGNAL	3M PIN NO.
UU	CH #1 SIGNAL GND	1
VV	CH #1 SIGNAL GND	2
TT	CH #1 +5 Vdc	3
AA	CH #1 20 mA XMIT +	18 groen
KK	CH #1 20 mA XMIT -	10 zwart
K	CH #1 20 mA REC +	32 blauw
S	CH #1 20 mA REC -	26 rood

J2

BERG PIN NO.	SIGNAL	3M PIN NO.
UU	CH #2 SIGNAL GND	1
VV	CH #2 SIGNAL GND	2
TT	CH #2 +5 Vdc	3
AA	CH #2 20 mA XMIT +	18
KK	CH #2 20 mA XMIT -	10
K	CH #2 20 mA REC +	32
S	CH #2 20 mA REC -	26

J3

BERG PIN NO.	SIGNAL	3M PIN NO.
UU	CH #3 SIGNAL GND	1
VV	CH #3 SIGNAL GND	2
TT	CH #3 +5 Vdc	3
AA	CH #3 20 mA Xmit +	18
KK	CH #3 20 mA XMIT -	10
K	CH #3 20 mA Rec +	32
S	CH #3 20 mA REC -	26

J4

BERG PIN NO.	SIGNAL	3M PIN NO.
UU	CH #4 SIGNAL GND	1
VV	CH #4 SIGNAL GND	2
TT	CH #4 +5 Vdc	3
AA	CH #4 20 mA Xmit +	18
KK	CH #4 20 mA Xmit -	10
K	CH #4 20 mA Rec +	32
S	CH #4 20 mA Rec -	26

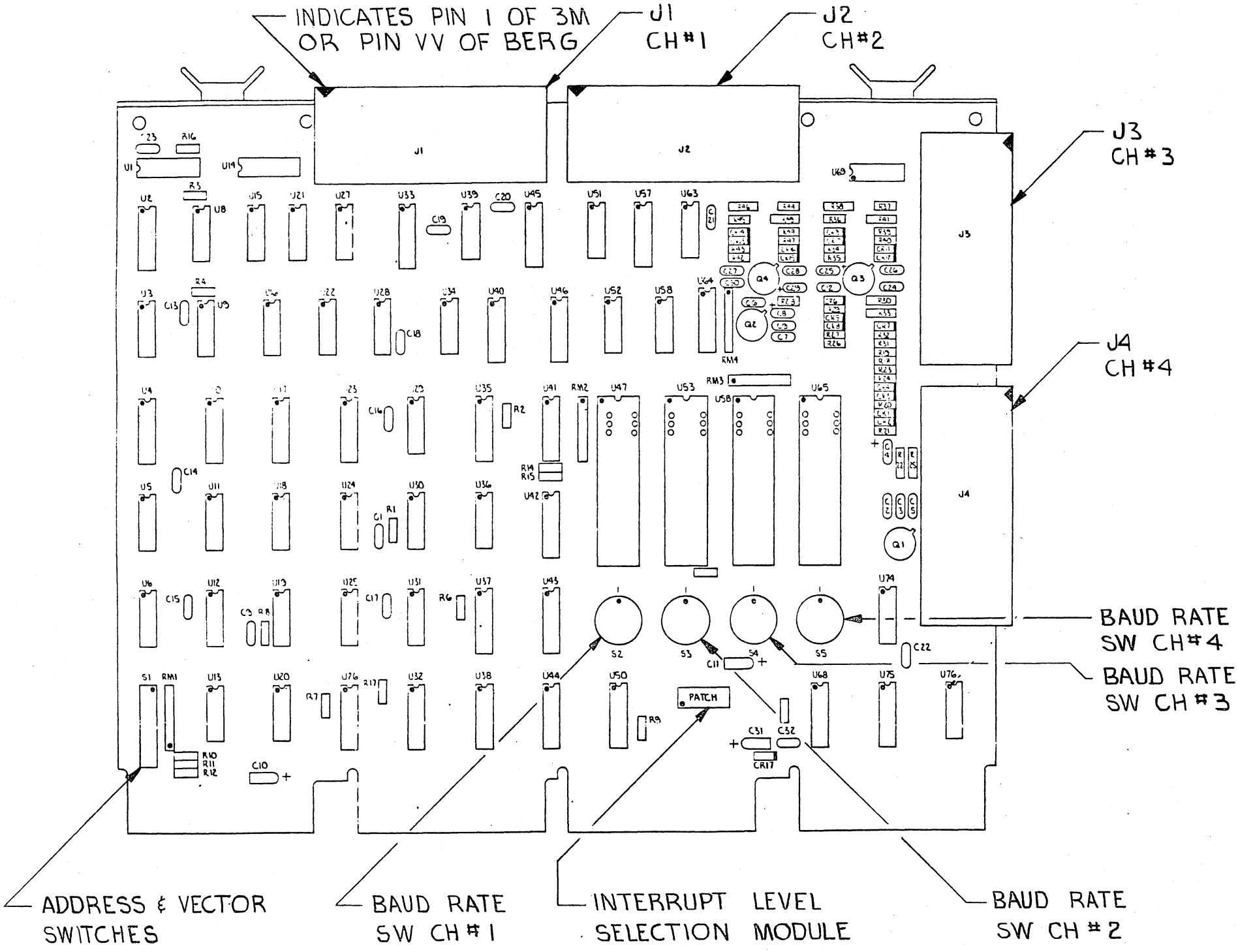
INTERRUPT LEVEL SELECTION

INTERRUPT LEVEL	JUMPER FROM					
	PIN 1	PIN 3	PIN 5	PIN 7	PIN 13	PIN 15
LEVEL 4	16	4	6	8	9	2
LEVEL 5	2	16	6	8	10	4
LEVEL 6	2	4	16	8	11	6
LEVEL 7	2	4	6	16	12	8

NOTE:

1) CONNECTION TO BE MADE BY JUMPER WIRES ADDED OR REMOVED ACCORDING TO THE ABOVE CHART.

2) NORMALLY SET FOR LEVEL 4.


INDICATES PIN 1 OF 3M OR PIN VV OF BERG
J1 CH#1
J2 CH#2
J3 CH#3
J4 CH#4
BAUD RATE SW CH#4
BAUD RATE SW CH#3
ADDRESS & VECTOR SWITCHES
BAUD RATE SW CH#1
INTERRUPT LEVEL SELECTION MODULE
BAUD RATE SW CH#2
PATCH